

FIG. 1(a) is a perspective view of a first embodiment of the present invention. The device includes a substrate 1, a first layer 2, a second layer 3, a third layer 4, a fourth layer 5, a fifth layer 6, and a sixth layer 7. The first layer 2 is a thin layer of material. The second layer 3 is a thin layer of material. The third layer 4 is a thin layer of material. The fourth layer 5 is a thin layer of material. The fifth layer 6 is a thin layer of material. The sixth layer 7 is a thin layer of material. The device is formed by a series of steps or layers.

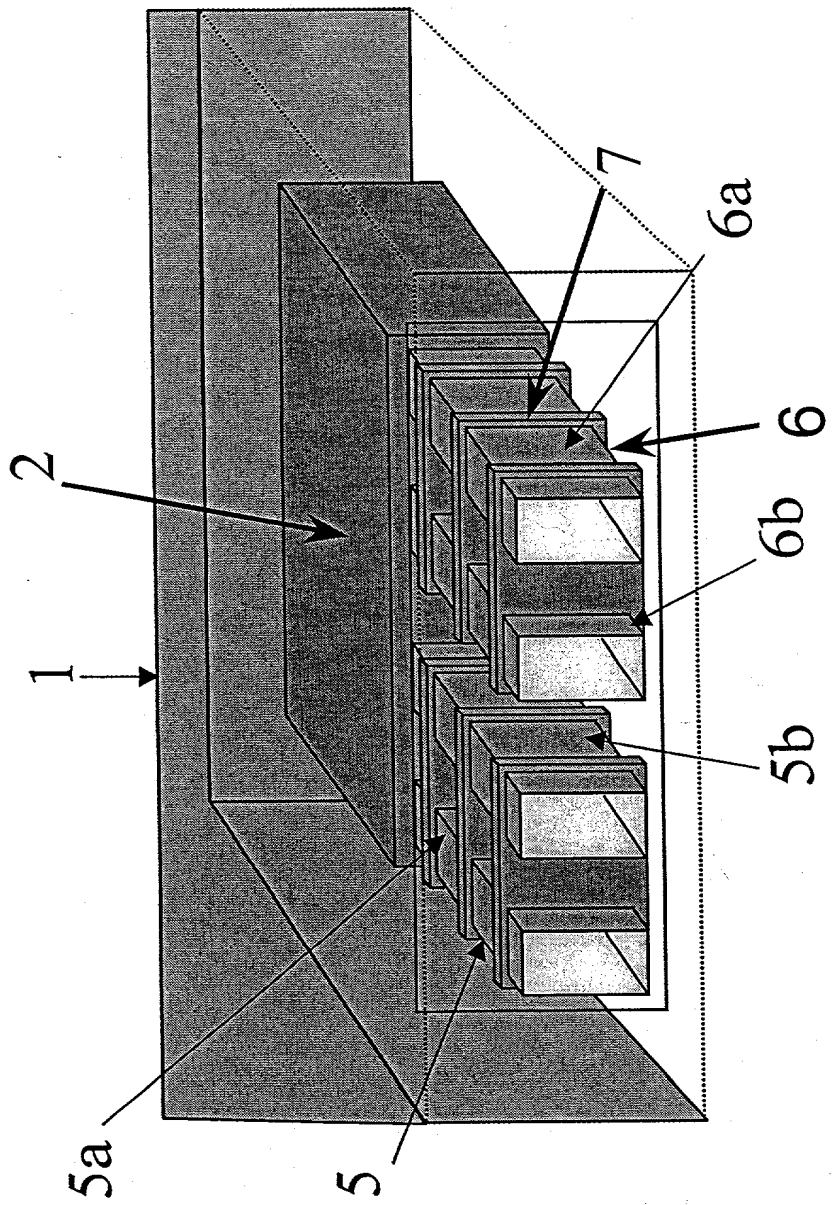
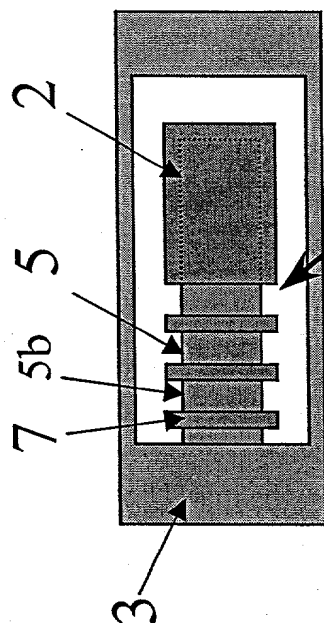
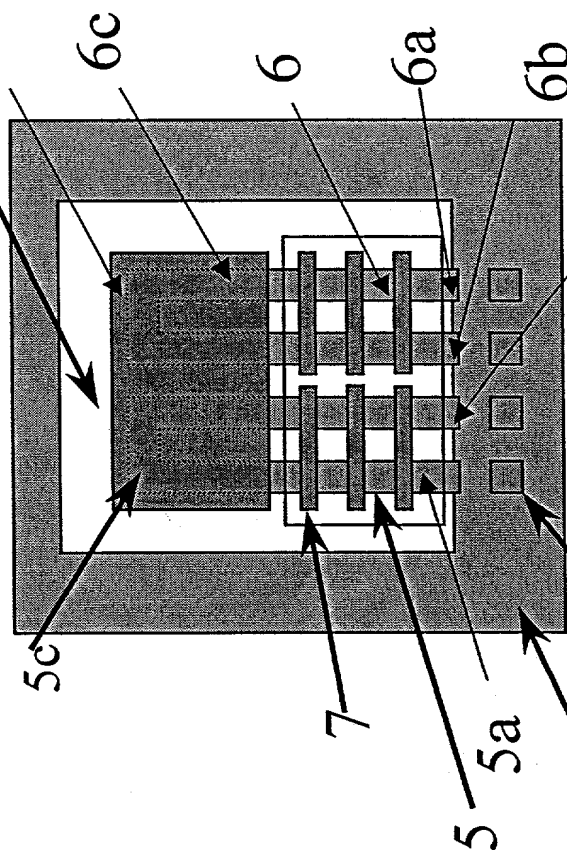


FIGURE 1(a)



**FIGURE 1(b)**



## 4/4 FIGURE 1(c) 5b

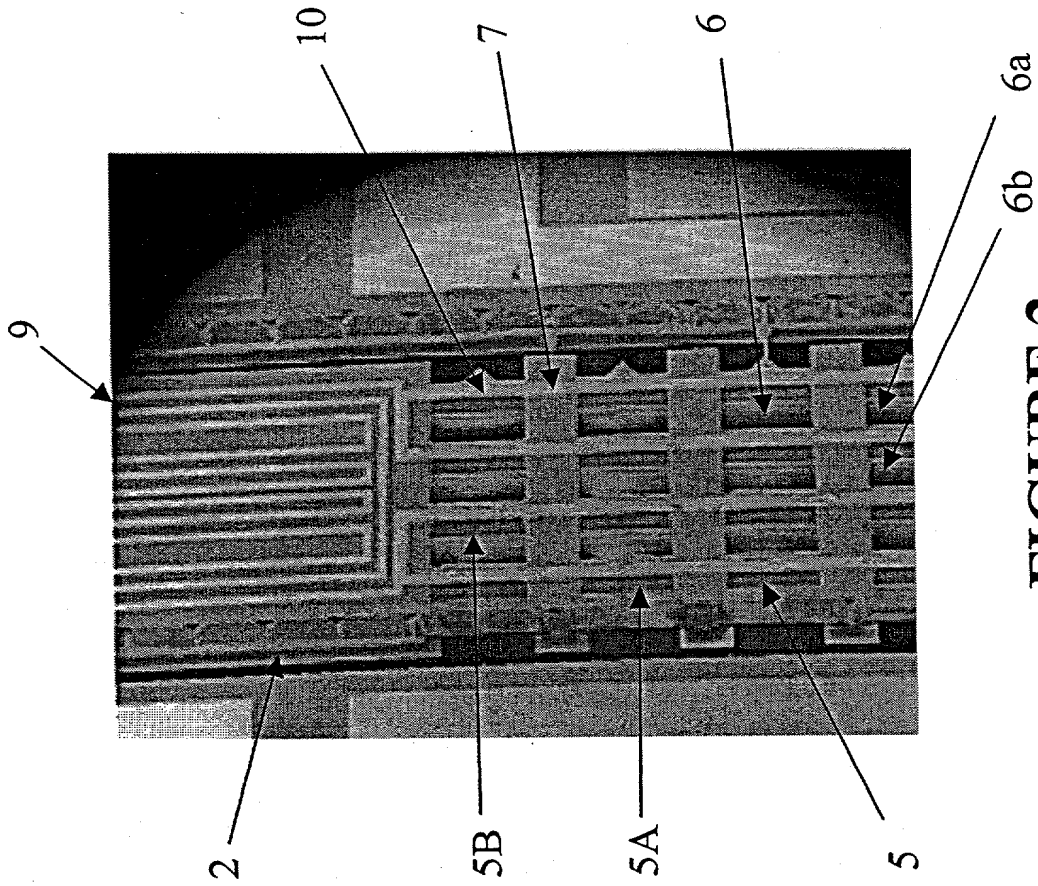
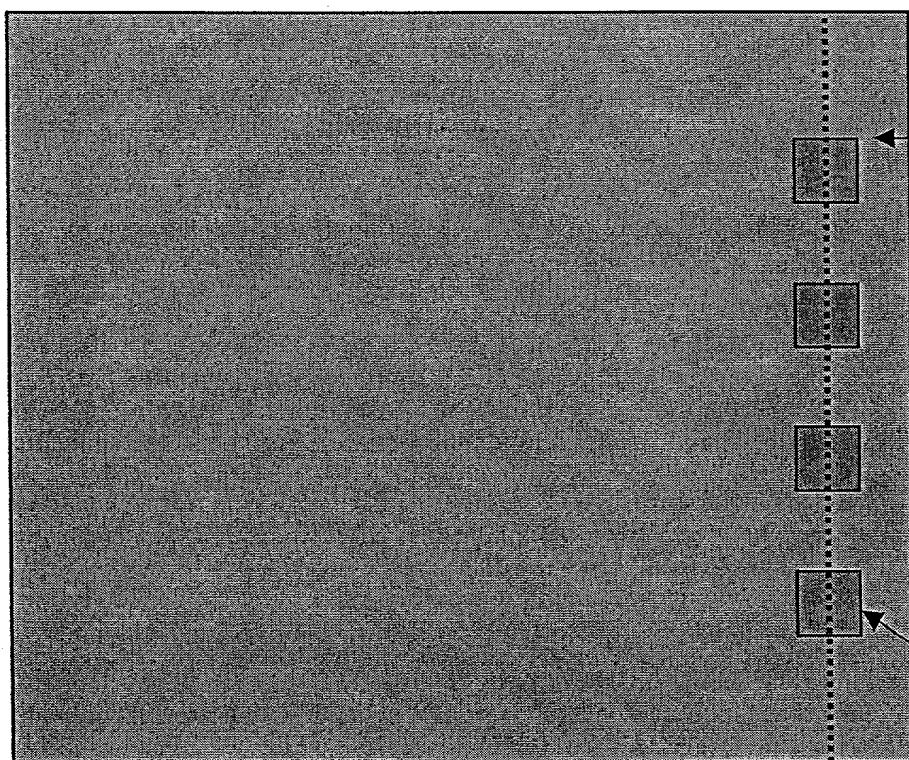


FIGURE 2







104 **FIGURE 5(a)** 103

FIG. 5(b) is a cross-sectional view of the device of FIG. 5(a) showing the device after the etching process. The device is shown in cross-section, with the substrate 103 and the etched regions 104. The etched regions 104 are shown as rectangular features on the surface of the substrate 103. The etching process is indicated by the arrows pointing to the etched regions 104.

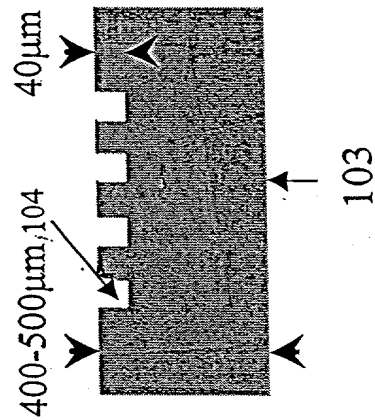
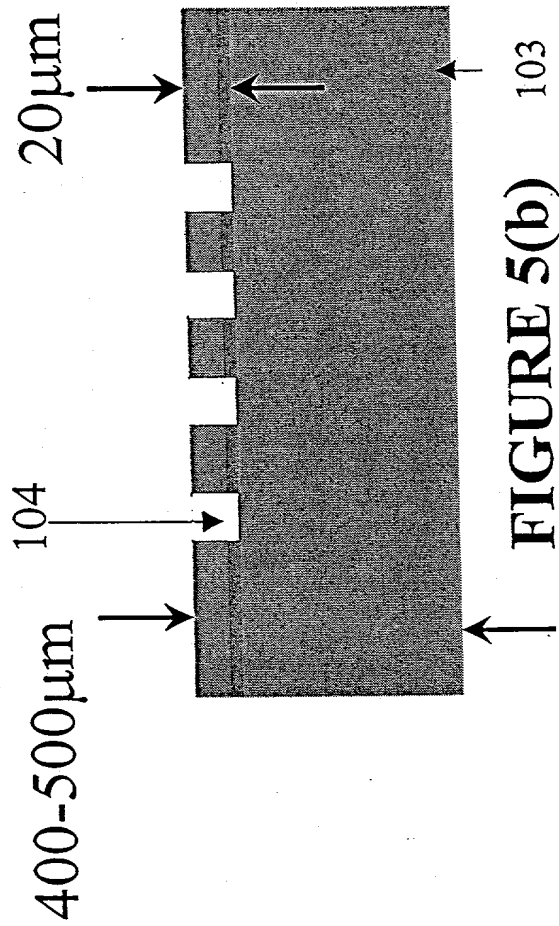


FIG. 5(d) is a plan view of a semiconductor device 100 showing a top view of a substrate 104 with a plurality of rectangular regions 106 arranged in a grid. The regions 106 are defined by a pattern of lines 108. A central region 110 is also shown, containing a pattern of lines 112. The regions 106 are labeled I, II, III, and IV, corresponding to the regions shown in FIG. 5(a). The regions 106 are arranged in a grid, with regions I and II in the top row, III and IV in the bottom row. The regions 106 are separated by lines 108. The central region 110 is surrounded by lines 112. The regions 106 are labeled I, II, III, and IV, corresponding to the regions shown in FIG. 5(a). The regions 106 are arranged in a grid, with regions I and II in the top row, III and IV in the bottom row. The regions 106 are separated by lines 108. The central region 110 is surrounded by lines 112.

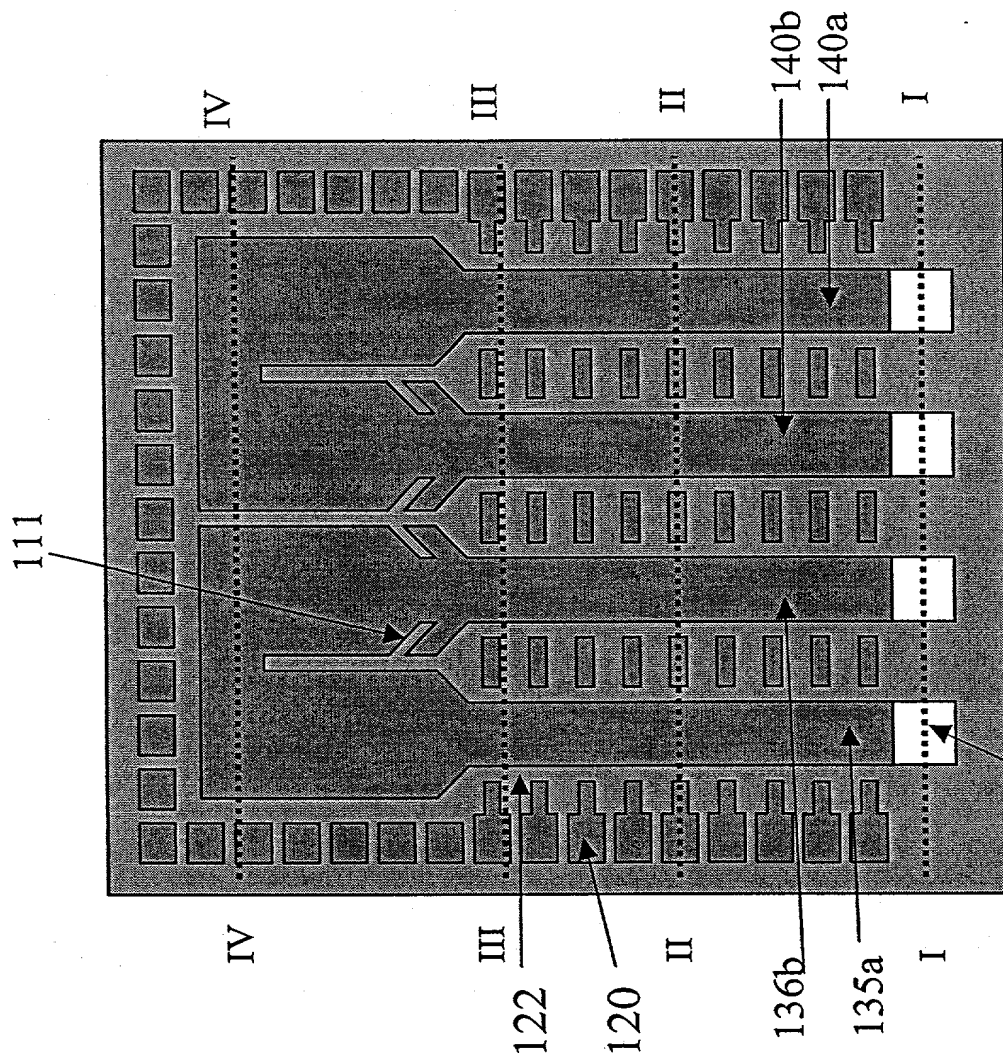
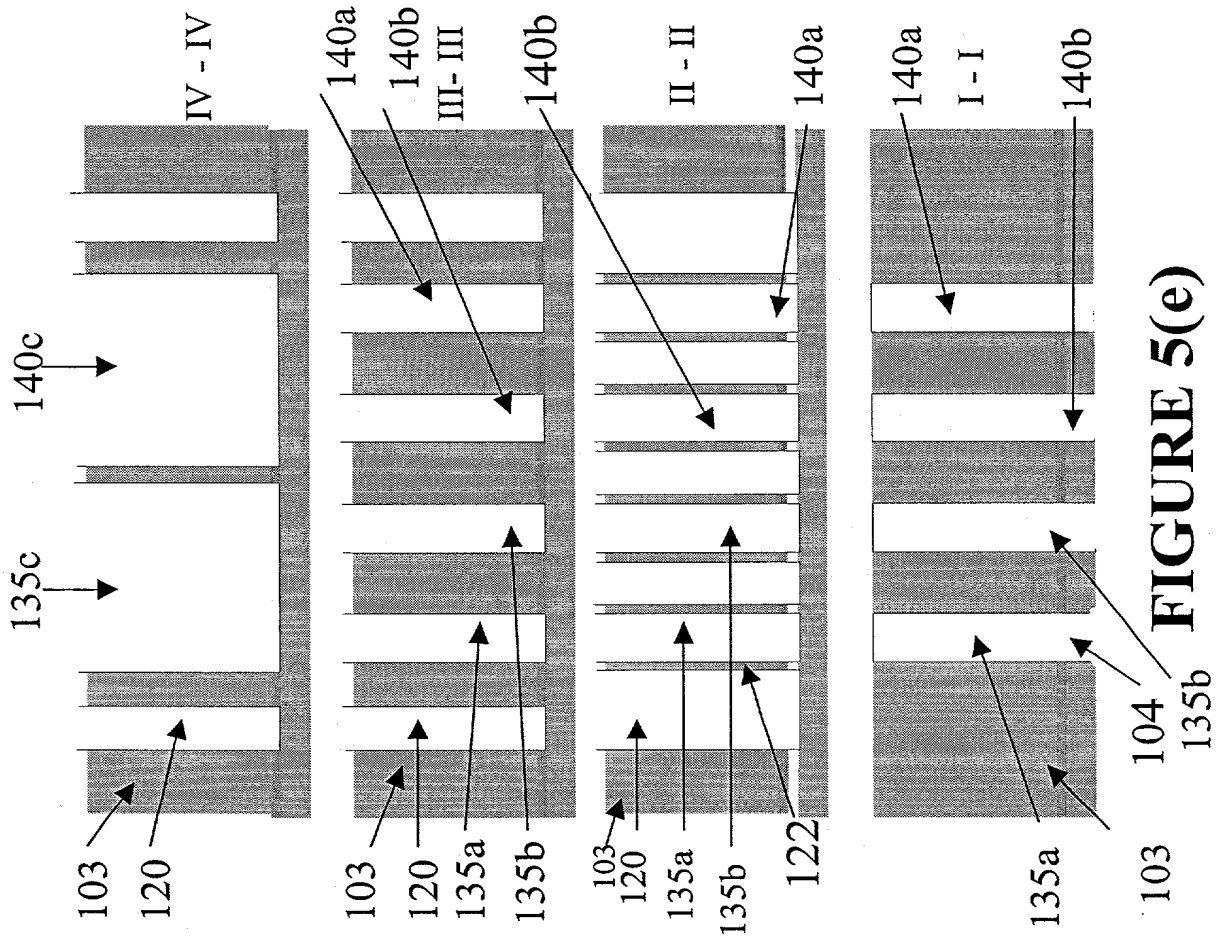


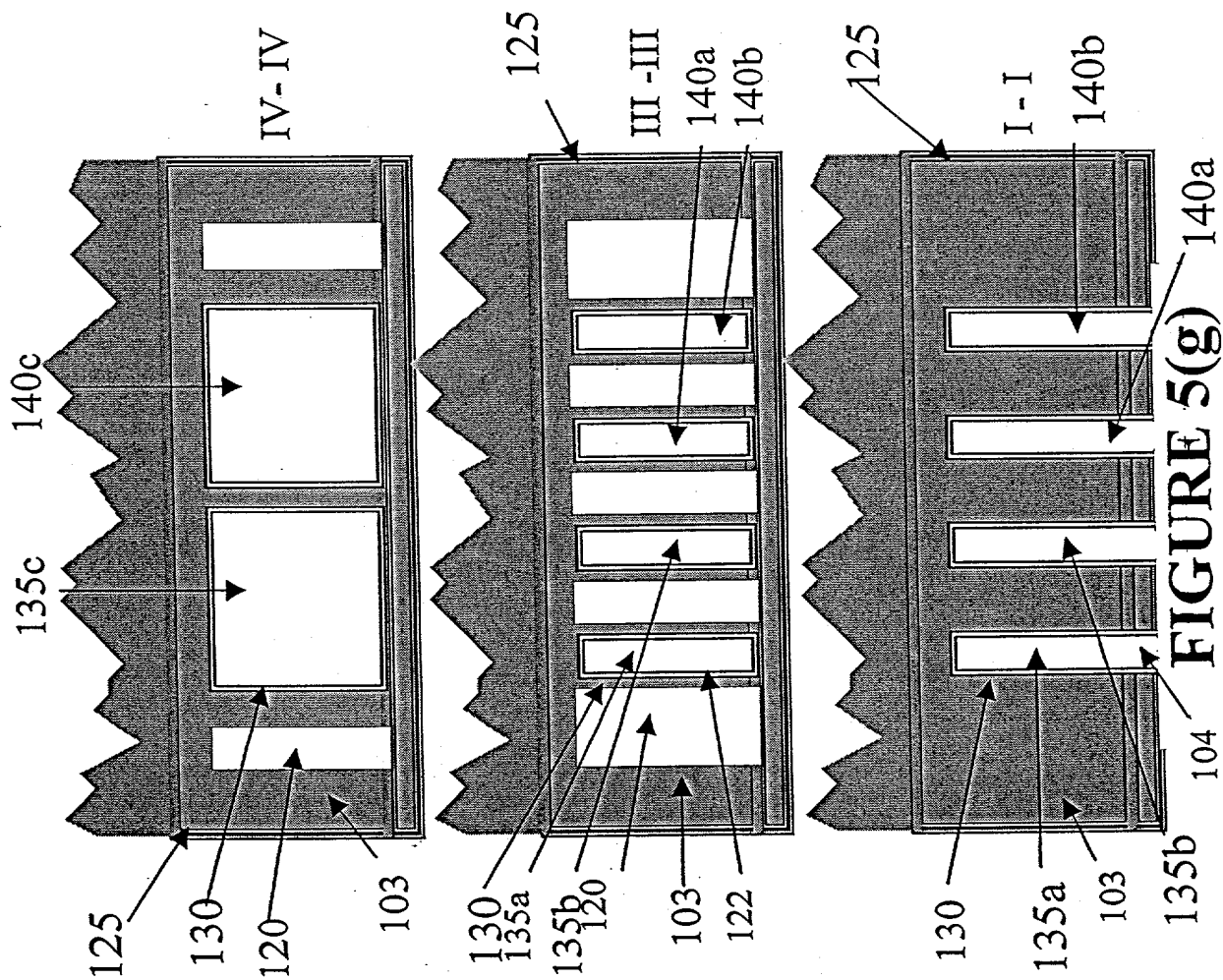
FIGURE 5(d)

104









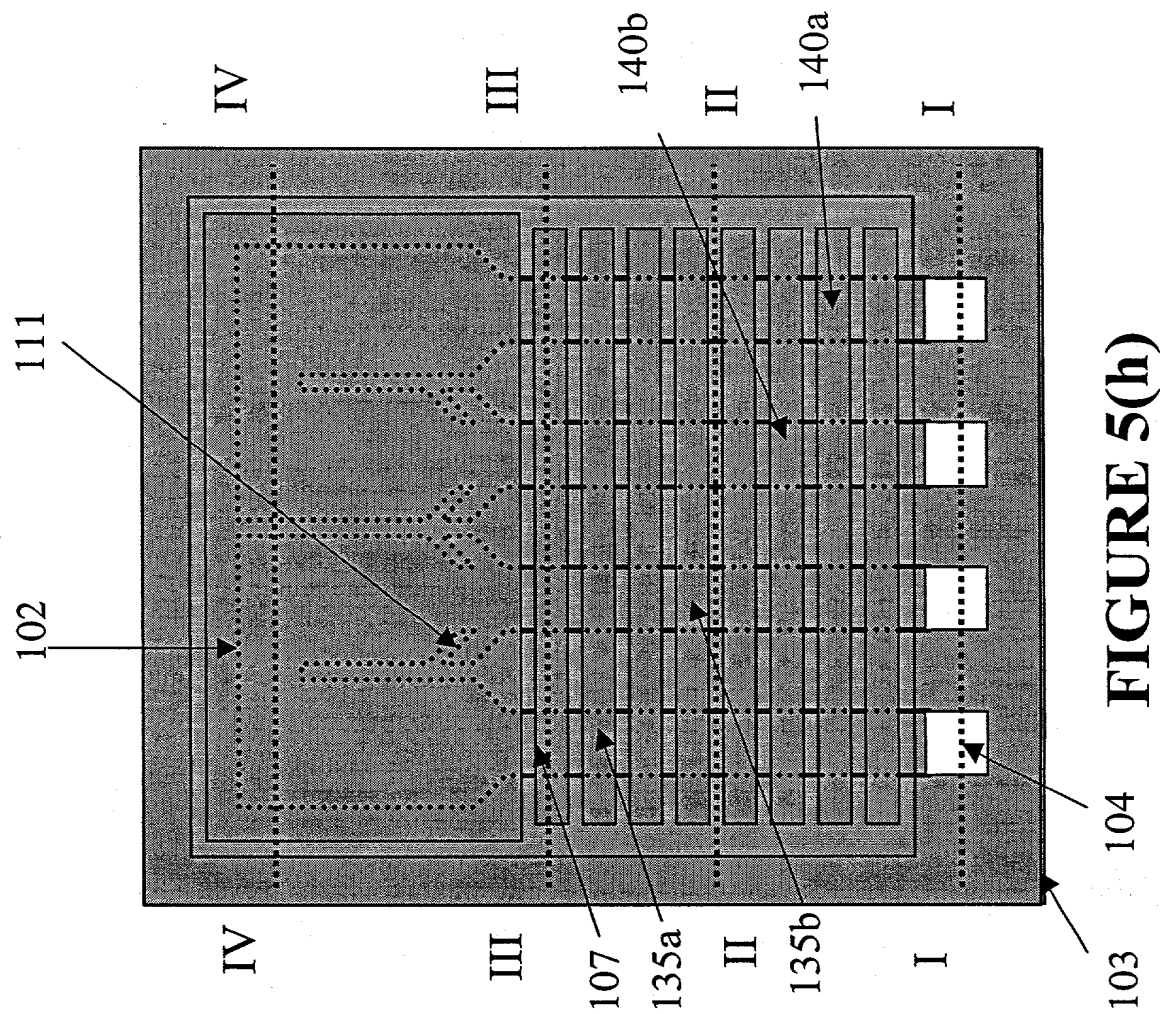


FIG. 5(i) is a cross-sectional view of the device 100 taken along line I-I of FIG. 5(h). The device 100 includes a substrate 102, a gate stack 103, a gate 104, a channel 105, a source/drain region 106, and a contact 107. The device 100 is configured to operate as a transistor.

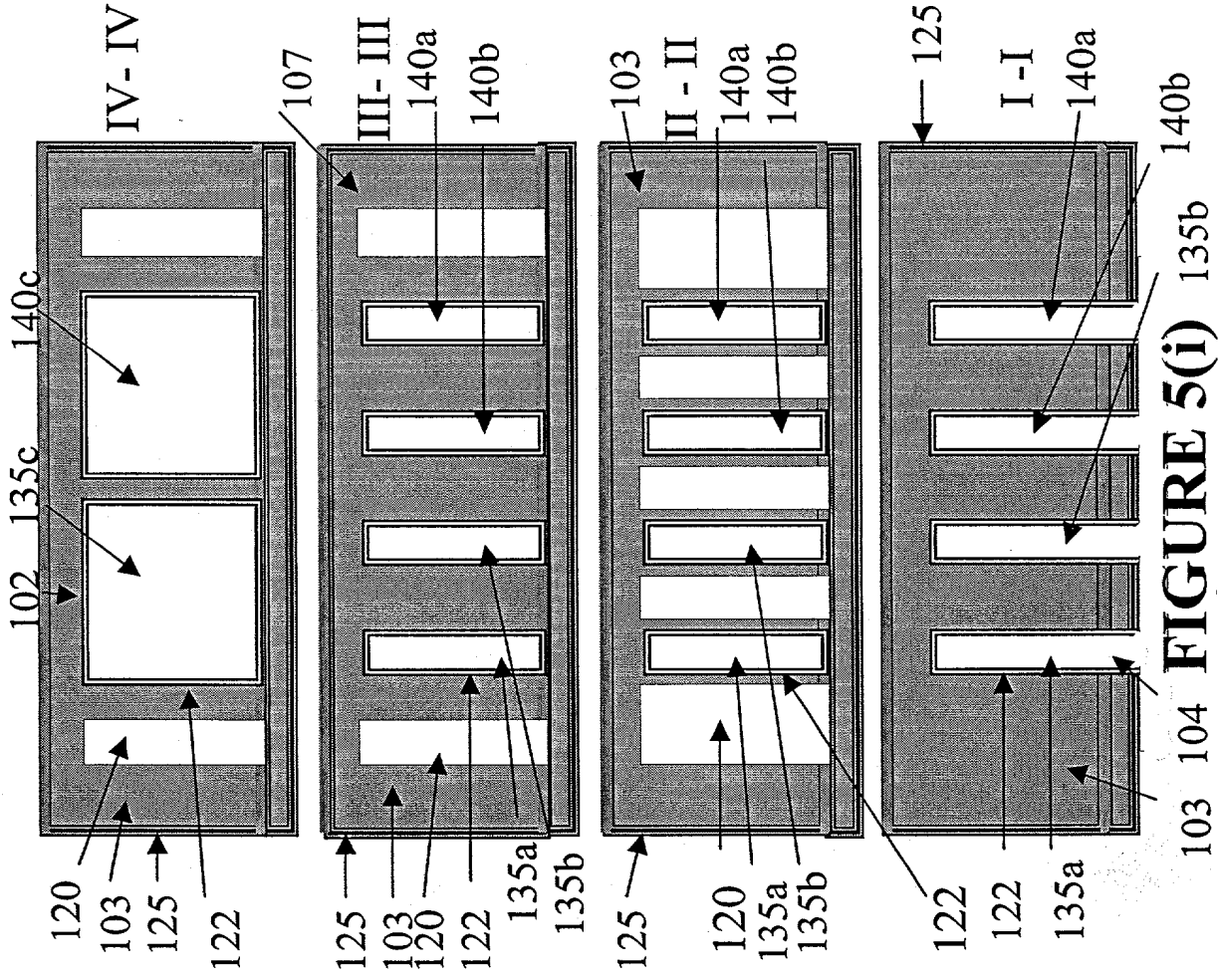




FIG. 5(k) is a cross-sectional view of the device of FIG. 5(j) taken along line 5-5 of FIG. 5(j). The device includes a substrate 103, a gate stack 104, and a channel layer 105. The gate stack 104 includes a gate dielectric layer 106a and a gate electrode layer 106b. The channel layer 105 is disposed on the substrate 103 and is in contact with the gate electrode layer 106b. The device also includes a source/drain region 107 and a contact layer 108. The source/drain region 107 is disposed on the channel layer 105 and is in contact with the contact layer 108. The contact layer 108 is disposed on the source/drain region 107 and is in contact with the gate electrode layer 106b. The device further includes a passivation layer 109 and a protective layer 110. The passivation layer 109 is disposed on the channel layer 105 and is in contact with the gate electrode layer 106b. The protective layer 110 is disposed on the passivation layer 109 and is in contact with the gate electrode layer 106b.

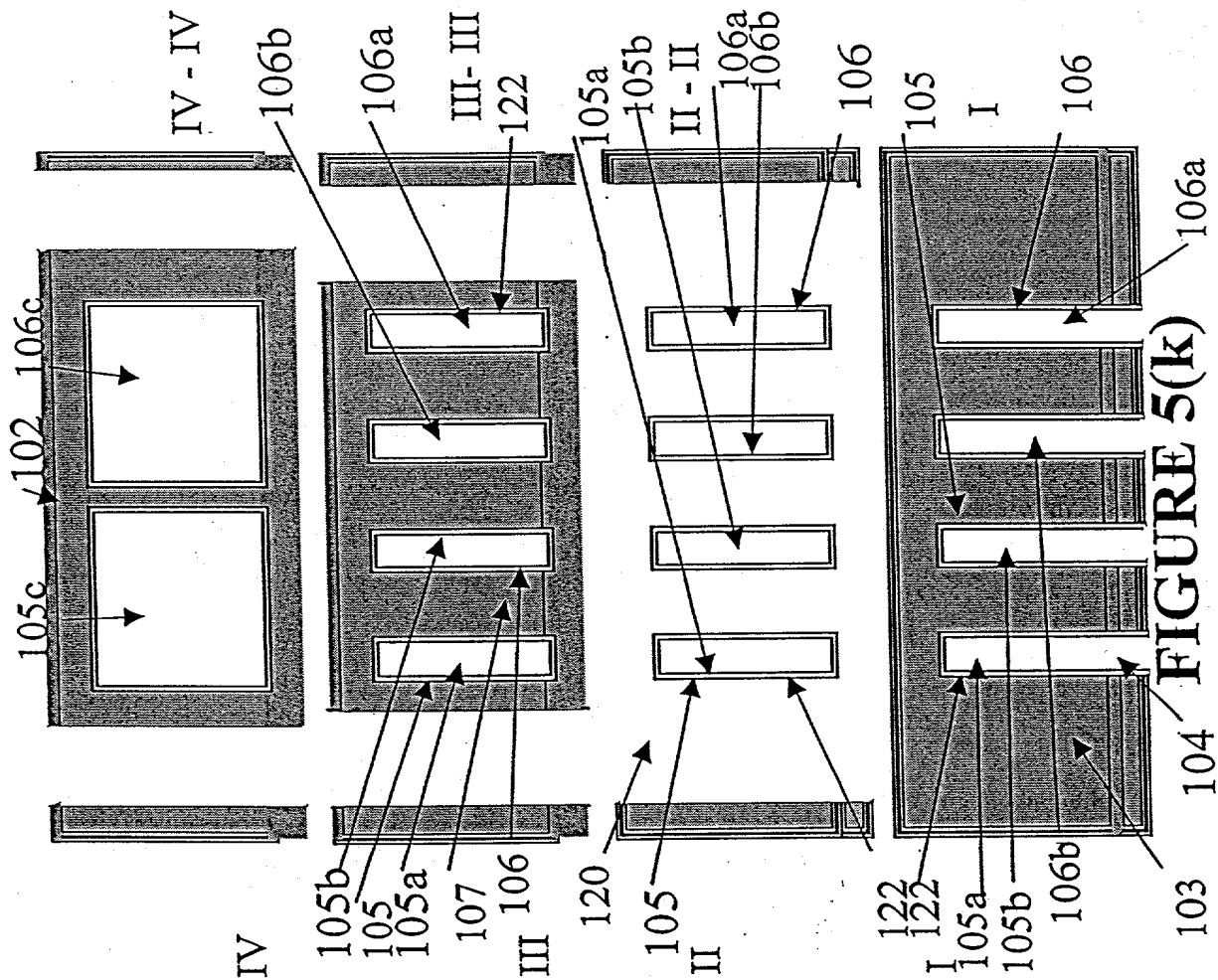
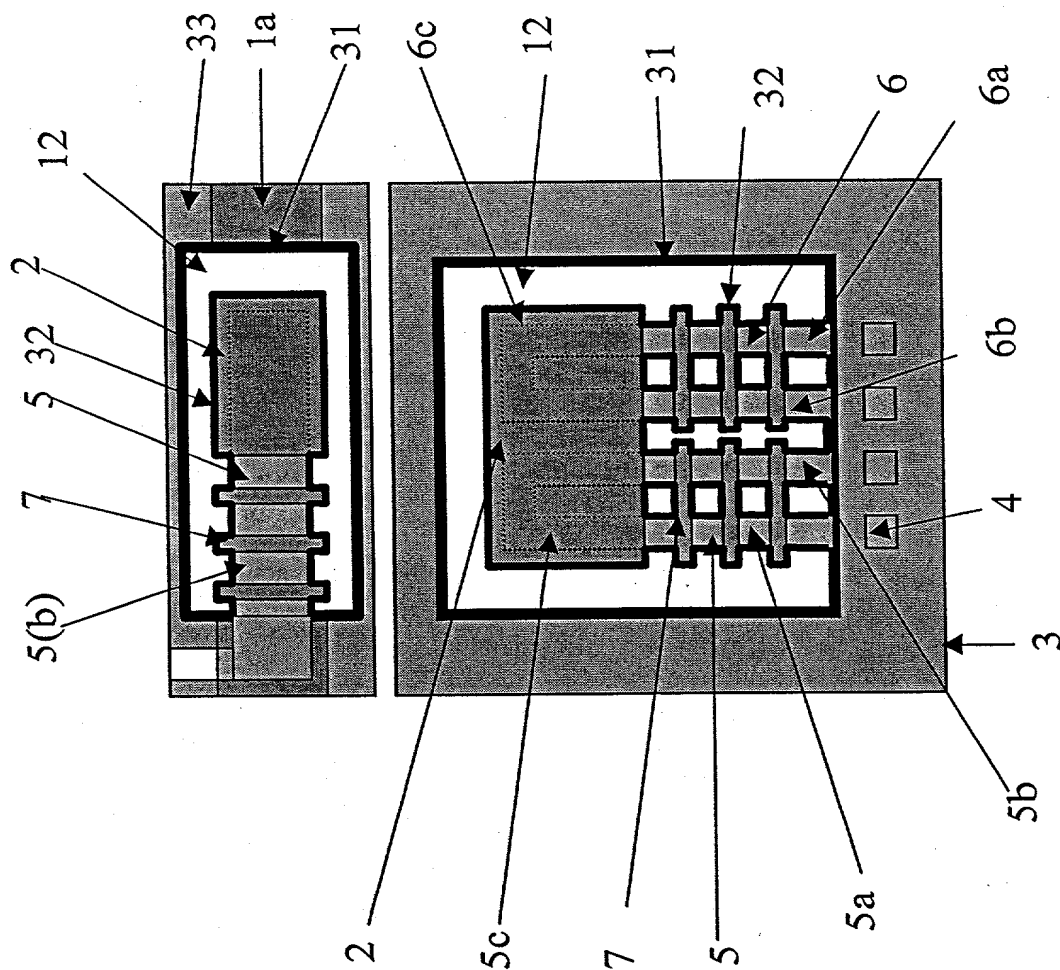
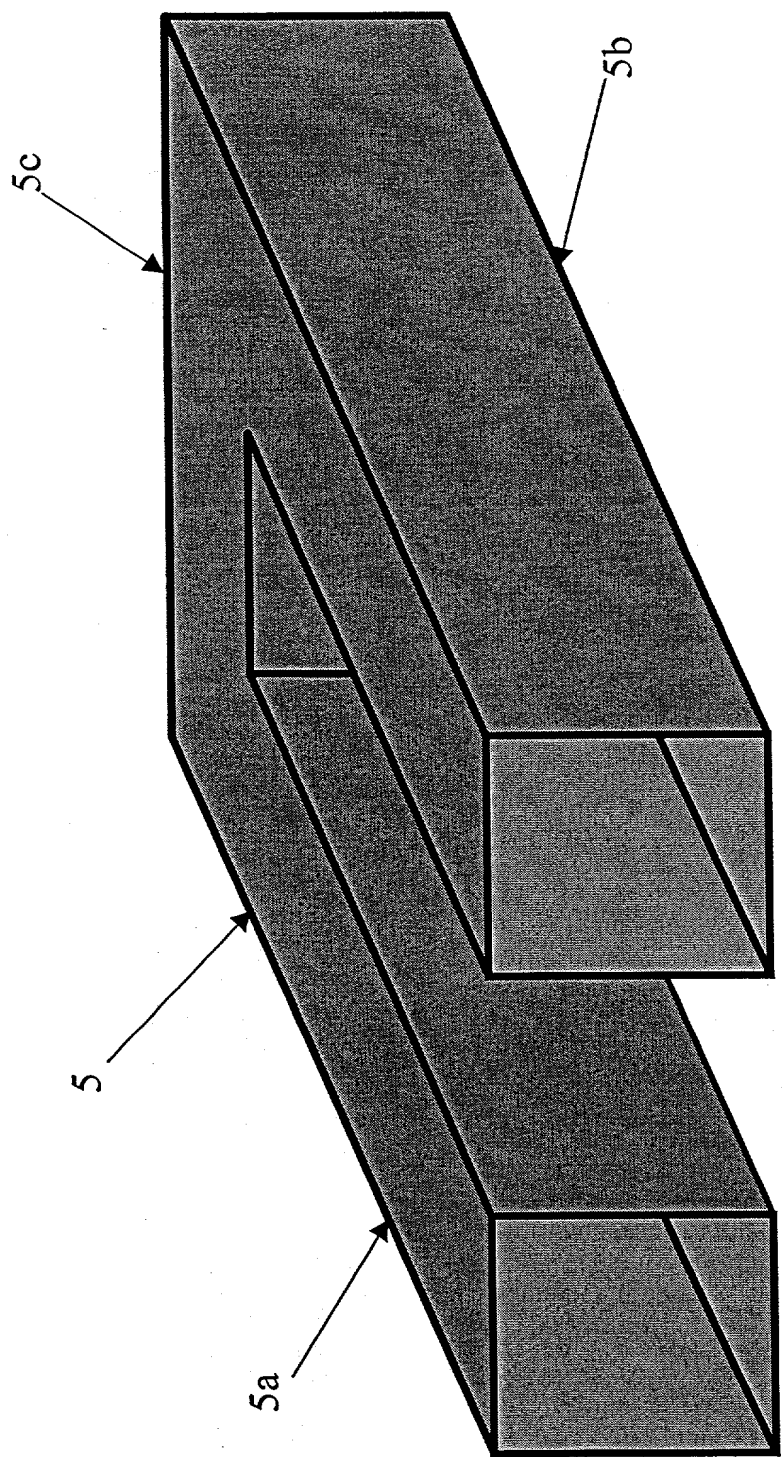


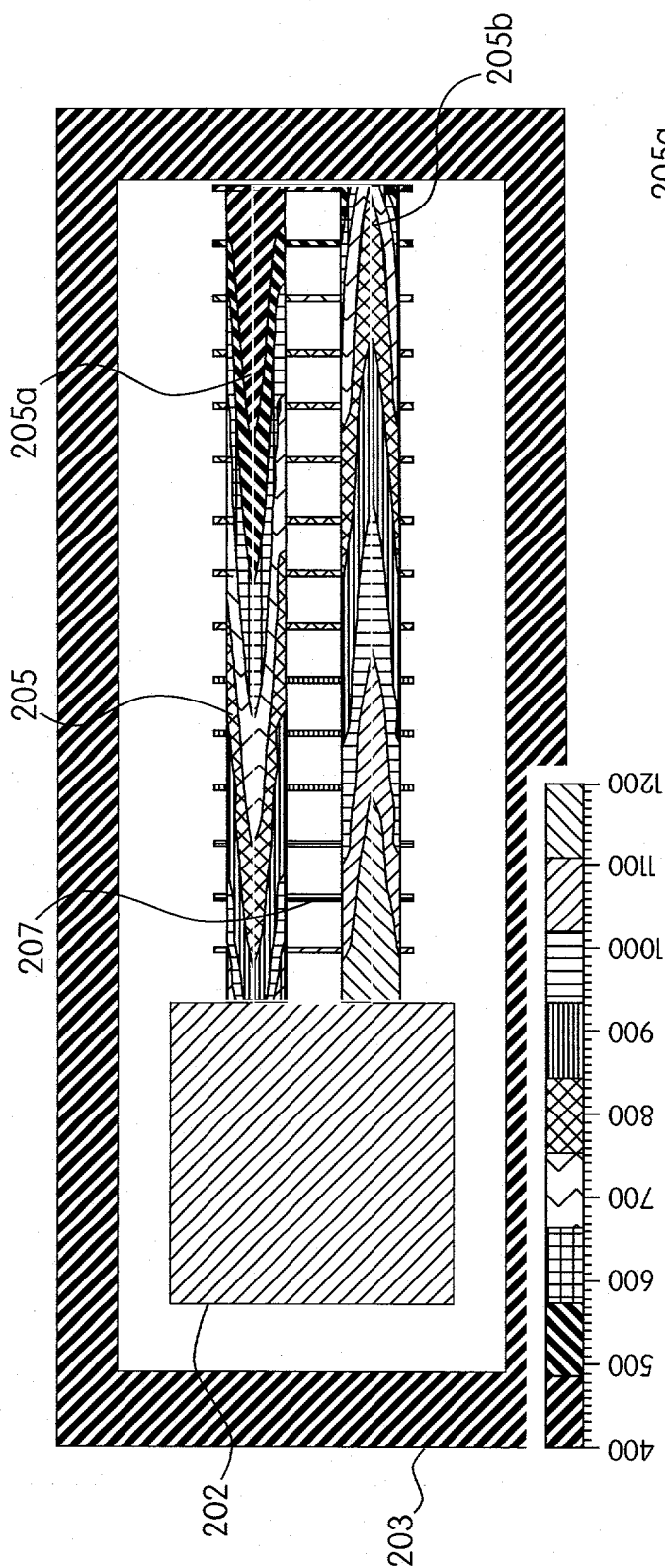
FIGURE 5(k)







# FIGURE 7



Temperature (C)

FIGURE 8a

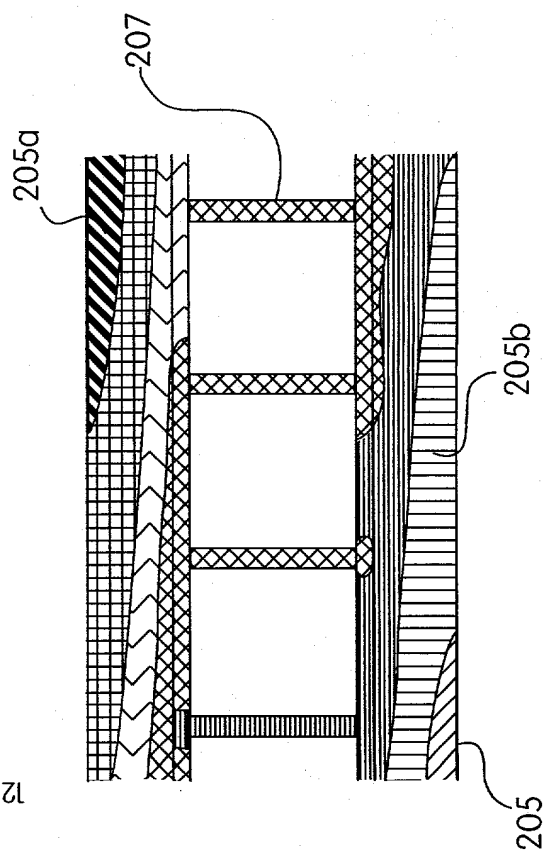
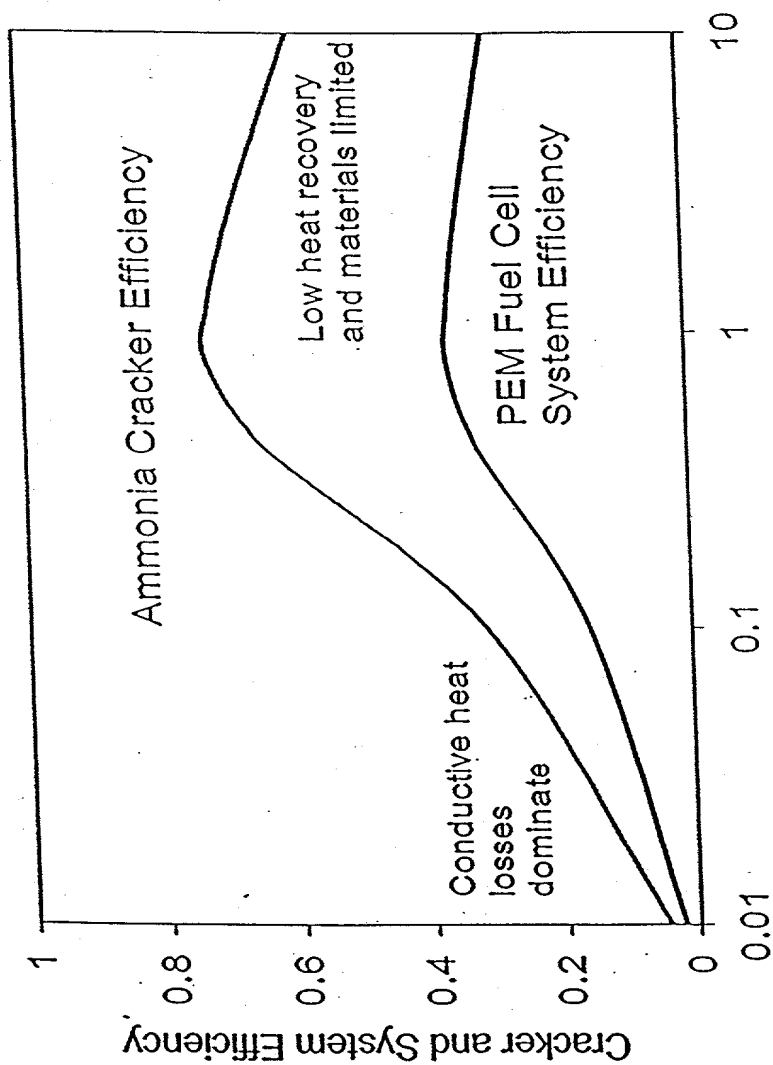
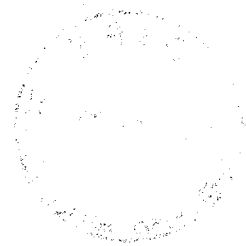


FIGURE 8b



System Power Output (w)

FIGURE 9



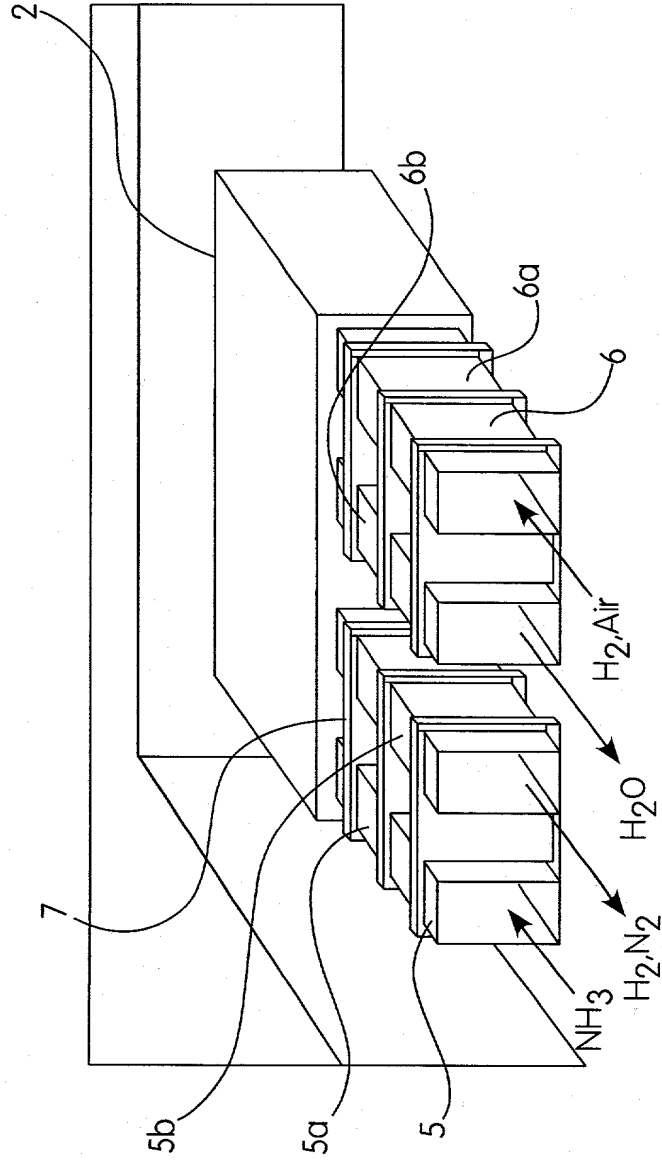


FIGURE 10a

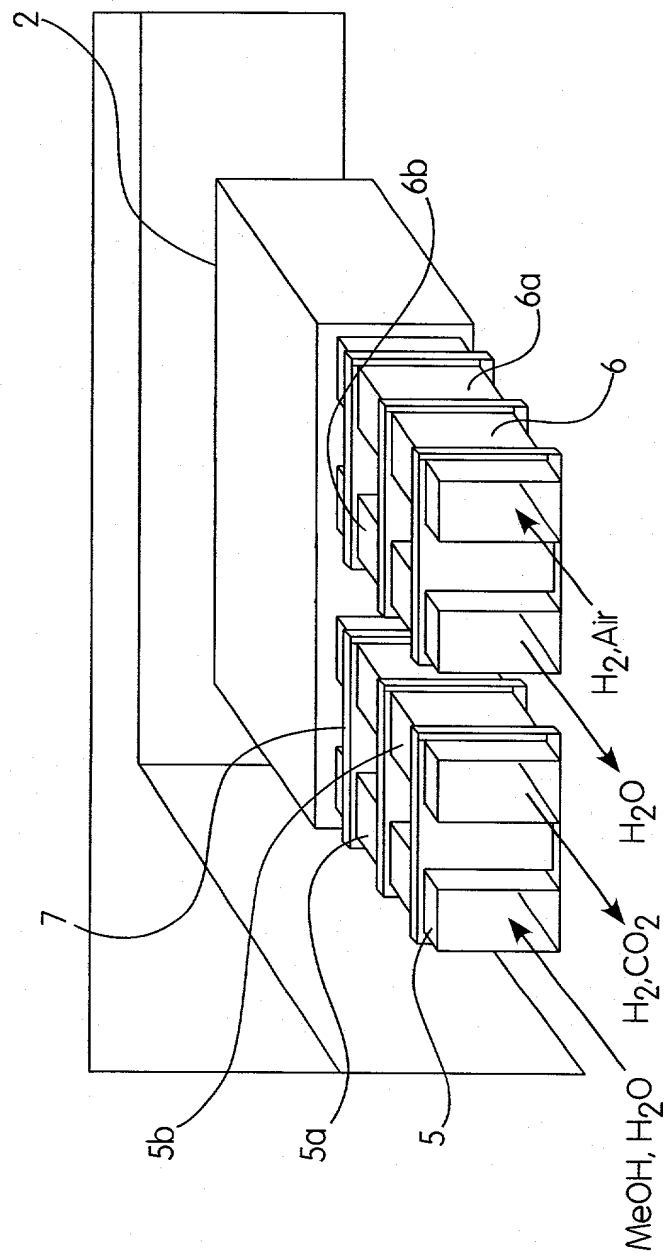


FIGURE 10b

FIG. 10C is a perspective view of the device 100 showing the fuel inlet 5, the air inlet 7, and the catalytic converter 2. The fuel inlet 5 is connected to a fuel source (not shown) and the air inlet 7 is connected to an air source (not shown). The catalytic converter 2 is located downstream of the fuel and air inlets. The device 100 is configured to convert the fuel and air into a gas mixture.

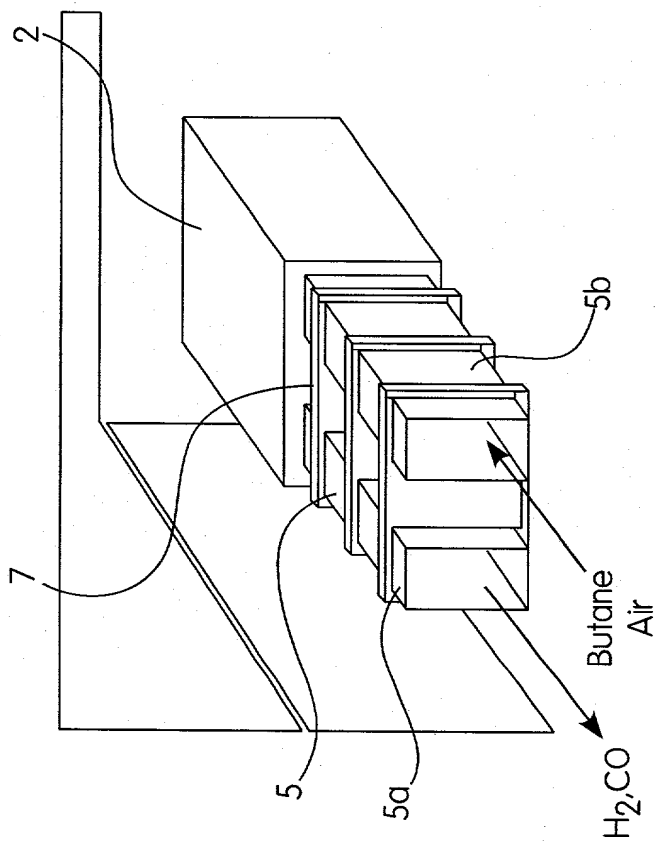


FIGURE 10c

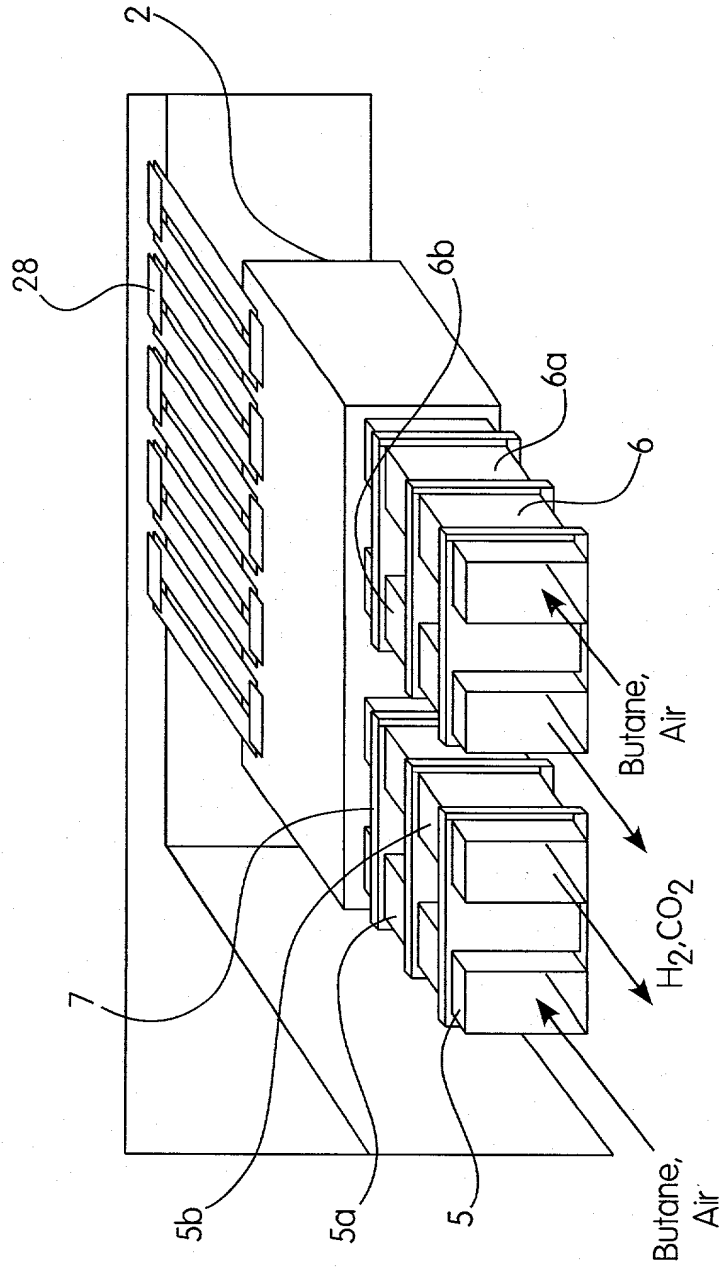
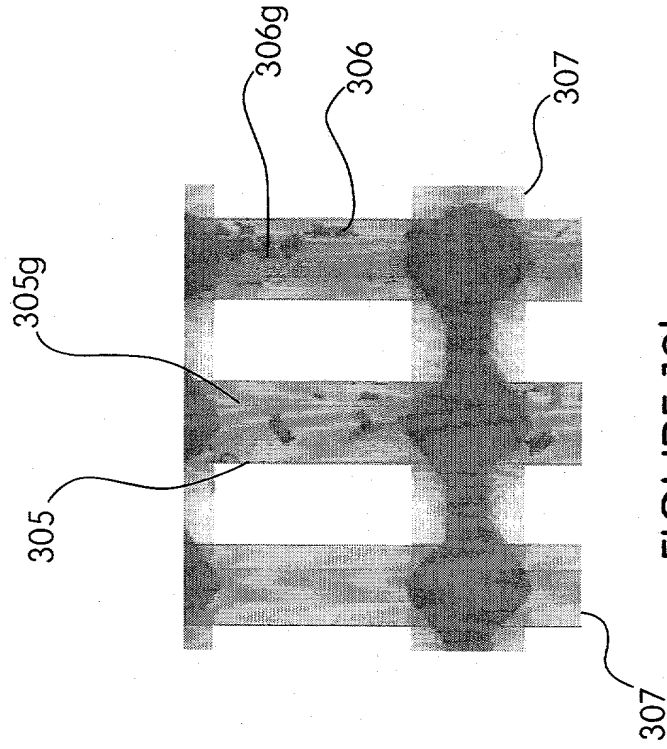
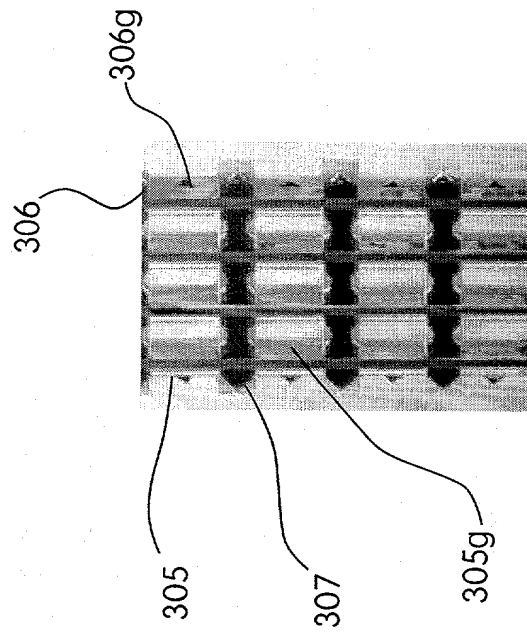


FIGURE 10d







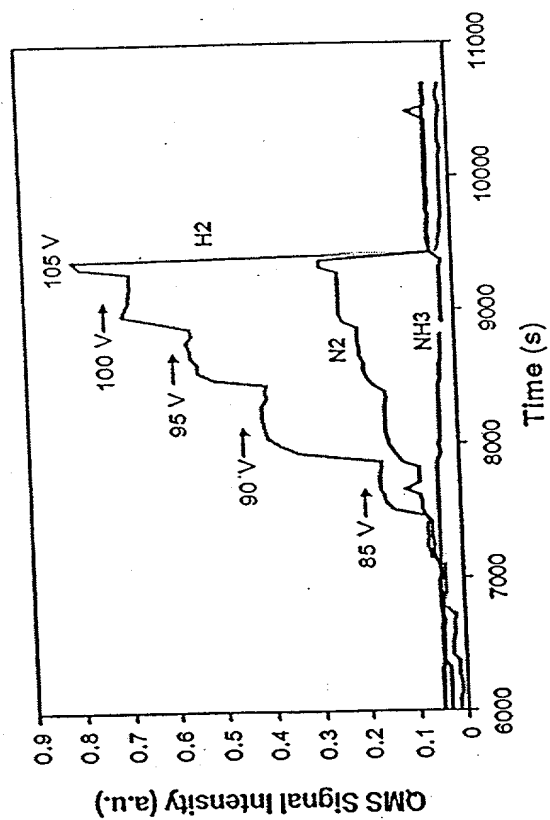


FIGURE 12(c)

